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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/675,525	09/29/2003	John Bruno	00100.03.0034	6091

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EXAMINER	
SUGENT, JAMES F	

ART UNIT	PAPER NUMBER
2116	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/675,525	BRUNO ET AL.	
	Examiner	Art Unit	
	James F. Sugent	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 April 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *12,13,15-19,34 and 44-47* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *12,13,15-19,34 and 44-46* is/are rejected.

7)☒ Claim(s) *47* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 April 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is sent in response to Applicant's Communication received April 20, 2007 for application number 10/675,525 originally filed September 29, 2003. The Office hereby acknowledges receipt of the following and placed of record in file: amended drawings (Figs. 2 and 4), amendments to the Specification, amended claims 1-47 (wherein claims 1-11, 14, 20-33, 35 and 36 have been canceled and claims 37-47 are new) are presented for examination.

Drawings

The new drawings to correct minor errors (Figs. 2 and 4) submitted, April 20, 2007, have been received, placed of record in file and accepted.

Specification

The amendments to the specification to correct minor errors (paragraphs 14 and 24) submitted, April 20, 2007, have been received, placed of record in file and accepted.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 17 and 18 are rejected under 35 U.S.C. 102(b) as being anticipated by Williams et al. (U.S. Patent No. 6,397,343 B1) (hereinafter referred to as Williams).

As to claim 17, Williams discloses in a system comprising a host processor and a graphics co-processor, a method for generating a clock signal for the graphics co-processor, the clock signal having an operating frequency set to a nominal operating frequency corresponding to a maximum rated junction temperature (Abstract and column 4, lines 29-64), the method comprising: detecting, by a thermal sensor (302) coupled to the graphics co-processor, a junction temperature corresponding to at least a portion of a circuit on a die constituting at least a portion of the graphics co-processor, thereby providing a temperature signal (column 9, lines 9-63 and column 10, lines 40-48); providing, by a thermal sensor control circuit (100) coupled to the thermal sensor (see Fig. 3), an interrupt control signal (104) and temperature data ("heat information from temperature sensor") in response to the temperature signal (column 9, lines 9-26 and column 10, lines 40-48); and, causing (via signal 106a), by the host processor (not shown but inherently present) coupled to the thermal sensor control circuit and in response to the interrupt control signal and the temperature data, an increase in the operating frequency of the clock signal above the nominal operating frequency (overclocking), when the detected junction temperature is below the maximum rated junction temperature (column 9, lines 27-63 and column 10, lines 16-48).

As to claim 18, Williams further discloses the method of claim 17 further including decreasing the operating frequency of the clock signal below the nominal operating frequency when the detected junction temperature is above the maximum rated junction temperature (column 12, lines 30-52).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 12, 13, 15, 16, 34, 37, 39, 40 and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bailey (U.S. Patent No. 5,451,892) (hereinafter referred to as Bailey) in view of Williams (as cited above).

As to claims 12 and 34, Bailey discloses clock control system for generating a clock signal having an operating frequency set to a nominal operating frequency corresponding to a maximum rated junction temperature (column 4, lines 20-40 and Fig. 1), comprising: a thermal sensor (134) operative to produce a temperature signal corresponding to a junction temperature of at least a portion of a circuit on a die (column 4, lines 57-66); a thermal sensor control circuit (130), operatively coupled to the thermal sensor, and operative to produce temperature data in response to the temperature signal and to provide an interrupt control signal (primary indicator

signal) in response to the temperature data (column 5, lines 28-46); a clock generator circuit (106) operative to produce the clock signal (column 4, lines 47-56); a dynamic frequency control data generator (120), operatively coupled to the thermal sensor control circuit and the clock generator circuit, and operative to provide dynamic frequency control data (control 162) to the clock generator circuit in response to the interrupt control signal and the received temperature data (column 4, line 67 and column 5, line 20); and, memory (136) comprising data representing junction temperatures over a temperature operating range with corresponding clock signal frequencies (column 5, lines 28-46 and column 5, line 62 thru column 6, line 17).

Bailey does not disclose the clock generator circuit increasing the operating frequency of the clock signal above the nominal operating frequency, when the detected junction temperature is less than the maximum rated junction temperature.

Williams teaches a clock control arrangement based upon temperature thresholds and clock frequencies for dynamically adjusting processor frequency (column 4, lines 29-64). Williams further teaches a clock generator circuit increasing the operating frequency of the clock signal above the nominal operating frequency (overclocking), when the detected junction temperature is less than the maximum rated junction temperature (column 10, lines 16-48). Williams has the additional benefit of maintaining low cost and complexity to a computer system (column 3, lines 35-56).

It would have been obvious to one of ordinary skill of the art having the teachings of Bailey and Williams at the time the invention was made, to modify dynamic clock method of Bailey to include exceeding a processor's nominal operating frequency according to a temperature threshold as taught by Williams. One of ordinary skill in the art would be motivated

to make this combination of exceeding a processor's nominal operating frequency according to a temperature threshold in view of the teachings of Williams, as doing so would give the added benefit of maintaining low cost and complexity to a computer system (as taught by Williams above).

As to claim 13, Bailey in combination with Williams taught the method in claim 12, as shown above. Bailey further teaches the method wherein the dynamic overclock frequency control data generator is operative to provide hysteresis based frequency control to increase the operating frequency of the clock signal above the nominal operating frequency if the detected junction temperature is below a lower junction temperature threshold, and the temperature dependent dynamic overclock generator circuit decreases the operating frequency of the clock signal below the nominal operating frequency if the detected junction temperature is above an upper junction temperature threshold wherein the upper junction temperature threshold is greater than the lower junction temperature threshold (column 5, lines 28-46).

As to claim 15, Bailey in combination with Williams taught the method in claim 12, as shown above. Bailey further teaches the method wherein the thermal sensor control circuit is operative to produce the interrupt control signal in response to a comparison between the temperature data and threshold temperature data (column 5, lines 28-46).

As to claim 16, Bailey in combination with Williams taught the method in claim 12, as shown above. Williams further teaches the method wherein the dynamic overclock frequency control data generator is operative to reduce at least one of: the frequency of the clock signal and a supply voltage to at least the portion of the circuit on the die in response to the interrupt control

signal and if the detected junction temperature is above a junction temperature threshold (column 10, lines 16-48).

As to claim 37, Bailey in combination with Williams taught the method in claim 16, as shown above. Williams further teaches the method wherein the junction temperature threshold is the maximum rated junction temperature (column 10, lines 16-48).

As to claim 39, Bailey in combination with Williams taught the method in claim 34, as shown above. Williams further teaches the method includes decreasing the operating frequency of the clock signal below the nominal operating frequency when the detected junction temperature is above the maximum rated junction temperature (column 12, lines 30-52).

As to claim 40, Bailey in combination with Williams taught the method in claim 34, as shown above. Bailey further teaches the method wherein the thermal sensor control circuit is operative to produce the interrupt control signal in response to a comparison between the temperature data and threshold temperature data (column 5, lines 28-46)

As to claim 42, Bailey in combination with Williams taught the method in claim 34, as shown above. Bailey further teaches the method wherein the data representing at least one of the junction temperatures and corresponding clock signal frequencies are based on a qualification testing procedure and further includes a safety margin to avoid a thermal runaway condition (column 6, line 59 thru column 7, line 11).

Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Williams as applied to claim 19 above, and further in view of Bailey (as cited above).

As to claim 19, Bailey teaches a clock controlling method which includes providing hysteresis based frequency control by: decreasing the operating frequency of the clock signal if

the detected junction temperature is above an upper junction temperature threshold, and increasing the operating frequency of the clock signal if the detected junction temperature is below a lower junction temperature threshold wherein the upper junction temperature threshold is greater than the lower junction temperature threshold (column 5, lines 28-46). Bailey has the additional benefit of comprising additional power savings methods and control.

It would have been obvious to one of ordinary skill of the art having the teachings of Williams and Bailey at the time the invention was made, to modify method of Williams to include hysteresis based frequency control as taught by Bailey. One of ordinary skill in the art would be motivated to make this combination of including hysteresis based frequency control in view of the teachings of Bailey, as doing so would give the added benefit of comprising additional power savings methods and control (as taught by Williams above).

Claims 38, 43 and 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bailey in view of Williams as applied to claim 34 above, and further in view of Helms et al. (U.S. Patent No. 6,889,332 B2) (hereinafter referred to as Helms).

As to claims 38, 43 and 44, Helms teaches a temperature based frequency adjustment method for a processor wherein: data representing junction temperatures is organized as a lookup table (column 7, lines 20-43 and column 7, lines 59-64); frequency adjustment is responsive to temperature data and the processing load (column 3, line 42 thru column 4, line 9); and, supply voltage to the processor die is reduced as a result of the junction temperature (column 5, lines 6-8). Helms has the additional benefit of comprising additional power savings methods and control.

It would have been obvious to one of ordinary skill of the art having the teachings of Bailey, Williams and Helms at the time the invention was made, to modify method of Bailey to include the additional features shown above as taught by Helms. One of ordinary skill in the art would be motivated to make this combination of including said features in view of the teachings of Helms, as doing so would give the added benefit of comprising additional power savings methods and control (as taught by Helms above).

Claim 41 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bailey in view of Williams as applied to claim 34 above, and further in view of Meynard (U.S. Patent Publication No. 2003/0229816 A1) (hereinafter referred to as Meynard).

As to claim 41, Meynard teaches a processor overclocking method wherein adjustment of the clock frequency accounted for a predetermined physical installation of the circuit on the die (paragraph 48). Meynard also teaches the additional benefits of comprising further both power and performance management in addition to overclocking a processor.

It would have been obvious to one of ordinary skill of the art having the teachings of Bailey, Williams and Meynard at the time the invention was made, to modify method of Bailey to include the clock frequency adjustment accounting for a predetermined physical installation of the circuit on the die as taught by Meynard. One of ordinary skill in the art would be motivated to make this combination of including the clock frequency adjustment accounting for a predetermined physical installation of the circuit on the die in view of the teachings of Meynard, as doing so would give the added benefit of comprising further both power and performance management in addition to overclocking a processor (as taught by Meynard above).

Claims 45 and 46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bailey (as cited above) in view of Williams (as cited above) and in further view of Meynard (as cited above).

As to claim 45, Bailey discloses a thermal sensor (134) operative to detect a junction temperature corresponding to at least a portion of a circuit on a die (column 4, lines 57-66); a temperature dependent dynamic clock generator circuit (120), operatively coupled to the thermal sensor, and operative to increase the operating frequency of the clock signal, dependent on the detected junction temperature (column 4, line 67 and column 5, line 20); and, memory (136) comprising data representing junction temperatures over a temperature operating range with corresponding clock signal frequencies (column 5, lines 28-46 and column 5, line 62 thru column 6, line 17).

Bailey does not disclose the clock generator circuit increasing the operating frequency of the clock signal above the nominal operating frequency, when the detected junction temperature is below the maximum rated junction temperature.

Williams teaches a clock control arrangement based upon temperature thresholds and clock frequencies for dynamically adjusting processor frequency (column 4, lines 29-64). Williams further teaches a clock generator circuit increasing the operating frequency of the clock signal above the nominal operating frequency (overclocking), when the detected junction temperature is less than the maximum rated junction temperature (column 10, lines 16-48). Williams has the additional benefit of maintaining low cost and complexity to a computer system (column 3, lines 35-56).

It would have been obvious to one of ordinary skill of the art having the teachings of Bailey and Williams at the time the invention was made, to modify dynamic clock method of Bailey to include exceeding a processor's nominal operating frequency according to a temperature threshold as taught by Williams. One of ordinary skill in the art would be motivated to make this combination of exceeding a processor's nominal operating frequency according to a temperature threshold in view of the teachings of Williams, as doing so would give the added benefit of maintaining low cost and complexity to a computer system (as taught by Williams above).

Neither Bailey nor Williams teaches the clock frequency accounted for a predetermined physical installation of the circuit on the die.

Meynard teaches a processor overclocking method wherein adjustment of the clock frequency accounted for a predetermined physical installation of the circuit on the die (paragraph 48). Meynard also teaches the additional benefits of comprising further both power and performance management in addition to overclocking a processor.

It would have been obvious to one of ordinary skill of the art having the teachings of Bailey, Williams and Meynard at the time the invention was made, to modify method of Bailey to include the clock frequency adjustment accounting for a predetermined physical installation of the circuit on the die as taught by Meynard. One of ordinary skill in the art would be motivated to make this combination of including the clock frequency adjustment accounting for a predetermined physical installation of the circuit on the die in view of the teachings of Meynard, as doing so would give the added benefit of comprising further both power and performance management in addition to overclocking a processor (as taught by Meynard above).

As to claim 46, Bailey in combination with Williams and Meynard taught the method in claim 45, as shown above. Bailey further teaches the method wherein the data representing at least one of the junction temperatures and corresponding clock signal frequencies are based on a qualification testing procedure and further includes a safety margin to avoid a thermal runaway condition (column 6, line 59 thru column 7, line 11).

Response to Arguments

Applicant's arguments with respect to claims 12, 13, 15-19, 34 and 44-46 have been considered but are moot in view of the new ground(s) of rejection.

Also, having further taken Examiner's cited references Applicant's arguments into further consideration, arguments presented by the Applicant have been taken into further consideration but are not persuasive.

Allowable Subject Matter

Claim 47 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to James Sugent whose telephone number is (571) 272-5726. The Examiner can normally be reached on 8AM - 4PM.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Rehana Perveen can be reached on (571) 272-3676. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at (866) 217-9197 (toll-free). If you would

like assistance from a USPTO Customer Service Representative or access to the automated information system, call (800) 786-9199 (IN USA OR CANADA) or (571) 272-1000.

James F. Sugent
Patent Examiner, Art Unit 2116
July 5, 2007

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SUPERVISORY PATENT EXAMINER
7/9/07